ABSTRACT OF THE DISCLOSURE

Data reading speed of a DRAM is enhanced without causing an increase in the power consumption and in the chip area. To that end, when data is read, a pair of bit lines is precharged to a GND level, while a dummy cell is charged at a power supply voltage. Immediately after a word line and a dummy word line are activated and their respective potentials are increased by the threshold voltage of an access transistor, a main capacitor and a dummy capacitor are electrically connected to the bit lines, thereby allowing the data to fade in. The resultant potential difference between the pair of bit lines is detected and amplified by a sense amplifier, thereby enabling the data to be read. The capacitance of the dummy capacitor is about half of that of the main capacitor, so that the dummy capacitor can be precharged at the power supply voltage.